FMD68151
CMOS Liquid Crystal Display Driver

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PRELIMINARY DATA SHEET

Description

The FMD68151 is a CMOS Integrated Circuit configured to drive Liquid Crystal Displays in Direct (Static) mode. The FMD68151 provides the RC oscillator and dividers, the microcontroller serial interface, a data output for cascading, a backplane driver and 38-segment outputs.

LCDs have been found to have wide temperature range, optimum contrast and viewing angle when driven in Direct-mode. By using a non-multiplexed LCD driving method, the need for a large voltage supply or a voltage converter can be eliminated allowing the system to operate from a single supply.

The FMD68151 is a CMOS 38-segment low voltage LCD driver. The inputs are CMOS compatible. The FMD68151 can be powered from a single 5V supply (V_{SS}=V_{EE}=0V). For applications requiring larger LCD driving voltages, the V_{EE} pin can be biased with up to -3V. This device offers test inputs to ease finding opens and shorts as well as automatic blanking of the display if the supply is lost.

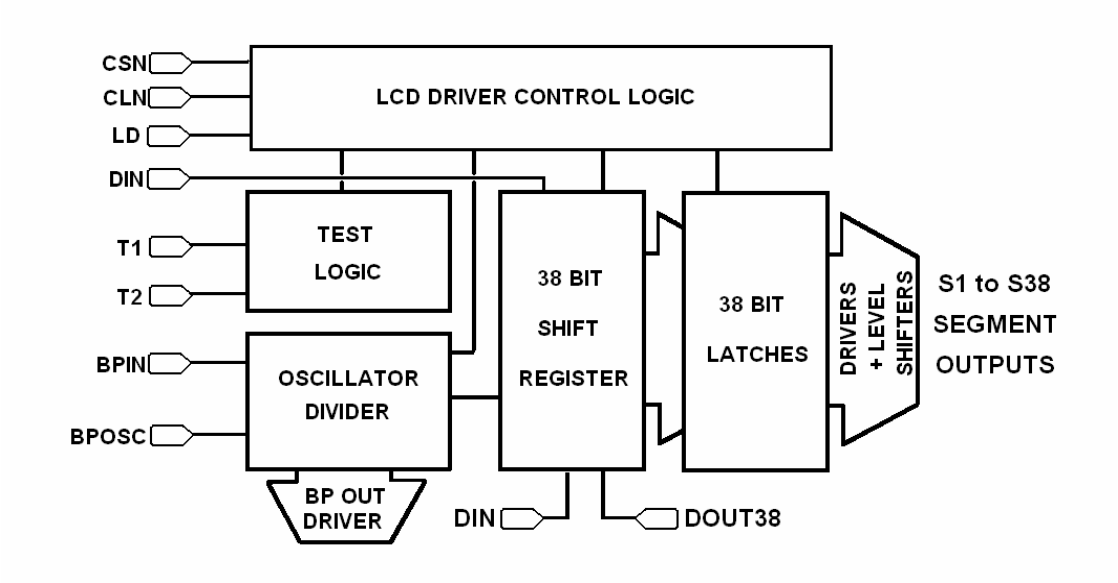
Data is serially clocked into the device on the negative edge of the clock (CLN) and latched in parallel to the segment outputs on the High to Low transition of the load (LD) input. For applications requiring more than 38 segments, cascading multiple devices is possible. The serial output data DOUT38 changes on the positive edge of the clock. Devices with DOUT32 or DOUT30 shift register data outputs are also available.

Other pinout configurations are available to match those with reverse logic on the Clock and Chip Select. Devices with only 32 segments equivalent to the MIC8030, MIC8031 and S4520 are also available.

Features

- **38 segment outputs**
- **Onboard RC oscillator or BP input clock when cascaded devices**
- **Cascadable (DOUT32 or DOUT30 SR data output options available)**
- **Built-in test inputs force outputs all “ON”, all “OFF” or alternating**
- **All segments forced to “OFF” if the positive supply is lost**
- **Supply Voltage 5V ± 10%**
- **LCD drive voltage range 5V to 8V (V_{DD}-V_{EE}) (Ideal for TN LCD applications)**
- **CMOS Low power**
- **Clock and Chip Select active low (Reverse logic option available)**
- **Functionally equivalent to HI8151/HI8050 and HI8010/HI8020(Low volt. applications)**
- **The 52-pin PQFP FMD68151 matches pin by pin the HI8151**

Block Diagram



Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNITS
Supply Voltage (V_{DD})	-0.3	7.0	
Supply Voltage (V_{EE})	-3.3		V
Storage Temperature	-55	+125	°C
Input Voltage (any Input)	V_{EE}-0.3	V_{DD} +0.3	V
Power Dissipation @ 85 °C		500	mW
Lead Soldering Temperature (10sec.)		280	°C

NOTE: Stresses above the absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operating at the limits is not recommended.

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITION
Supply Voltage (V_{DD} to V_{SS})	V_{DD}	+5V ± 10%
Supply Voltage (V_{EE} to V_{SS})	V_{EE}	0V or -3V ± 10%
Operating Temperature	T_A	-40°C to +85°C
Operating Frequency (Approx.)	F_{BP}	100 Hz
Resistor (Oscillator RC network)	R	220 kΩ
Capacitor (Oscillator RC network)	C	220 pF
Logic Input Levels	LD,CLN,CSN,DIN	0 to V_{DD}
BPIN Input (when cascading ICs)	BPIN	V_{EE} to V_{DD}

Electrical Characteristics

DC Electrical Test Specification

V_{DD} =5V ± 10%, V_{EE}=-3.0V ± 10%, VSS =0V, T_A =-40°C to +85°C (Unless otherwise specified).

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage	With respect to Vss	4.75		5.25	V
I_{DD}	Supply Current	Static, No load, V_{EE}=0		470		µA
V_{EE}	Supply Voltage	With respect to Vss	-3.3		0	V
I_{EE}	Supply Current	Static, No load, V_{EE}=0		230		µA
V_{IH}	Input High Voltage		0.7 V_{DD}			V
V_{IL}	Input Low Voltage				0.3 V_{DD}	V
V_{IHBPIN}	Input High Voltage for BPIN		0.8 V_{DD}			V
V_{ILBPIN}	Input Low Voltage for BPIN		V_{EE}		0.6 V_{DD}	V
I_{IH}	Input Current				100	nA
C_I	Input Capacitance				10	pF
R_{SEG}	Segment Output Impedance	I_L=10uA		470		Ω
R_{BP}	Backplane Output Impedance	I_L=10uA, @ 25°C		56		Ω
I_{DOH}	Data Output Current (Source)	V_{OH}= 4.5V			-3.0	mA
I_{DOL}	Data Output Current (Sink)	V_{OL}= 0.4V	3.2			mA
V_{OS}	Offset Voltage (BP to Seg.)	DC (0.16Hz Filter)			25	mV

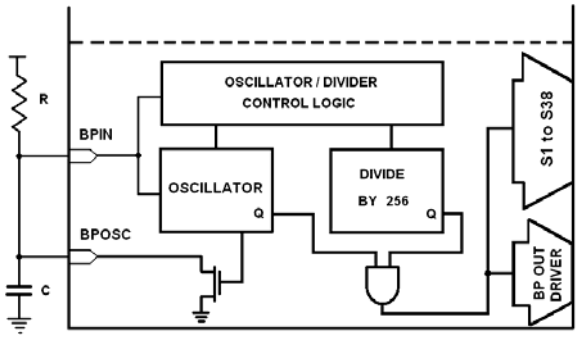
AC Electrical Characteristics

AC Electrical Test Specification

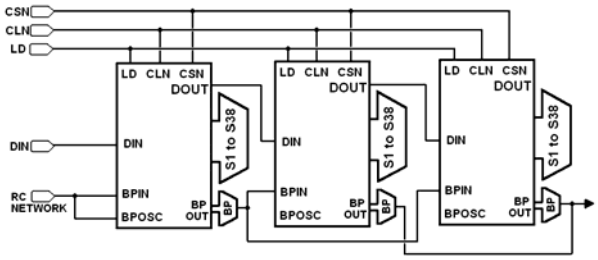
V_{DD} =5V ± 10%, V_{EE}=-3.0V ± 10%, VSS =0V, T_A =-40°C to +85°C (Unless otherwise specified).

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{CL}	Clock – Period	Non-cascaded	250			nS
t_{CL}	Clock – Period	Cascaded	500			nS
t_{CW}	Clock – Width	Non-cascaded	125			nS
t_{CW}	Clock – Width	Cascaded	250			nS
t_{SD}	Data In – Setup		50			nS
t_{HD}	Data In – Hold		80			nS
t_{SCS}	Chip Select – Setup to CLN		100			nS
t_{HCS}	Chip Select – Hold to CLN		120			nS
t_{SLD}	Load – Setup to CLN		120			nS
t_{SCSLD}	Chip Select – Setup to LD		0			nS
t_{WLD}	Load - Pulse Width		130			nS
t_{HCSLD}	Chip Select – Hold to LD		120			nS
t_{DV}	Data Valid - from CLN				170	nS

Internal Oscillator Circuit Hook-up (Figure 1)

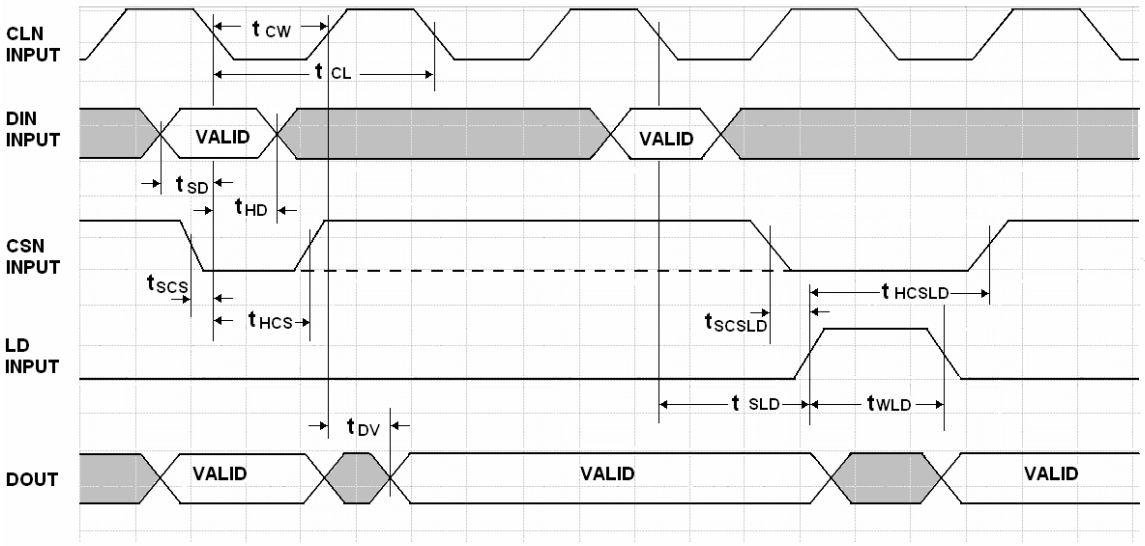


Cascading Multiple Devices with RC Osc.(Figure 2)



When cascading devices driven by an external clock, feed the same clock to all the BPINs.

Timing Diagrams (Figure 3)



Because Chip Select and Clock are AND together, it is recommended to bring CSN high when CLN is low. Otherwise, keep CSN low (dotted line) until LD is pulsed high then low before bringing CSN back high.

Pin Descriptions

PIN	SYMBOL	FUNCTION	DESCRIPTION
1	LD	Logic Input	Latches data in the shift register into the segment outputs (Active High)
2	DIN	Logic Input	Serial input data into the shift register
3	BPIN	Input	Segment and Backplane frequency input. Driven externally from a clock source or connected to BPOSC and an external RC.
4	BPOSC	Output	Internal OSC pin. Left open or connected to BPIN and an external RC.
5	VDD	Power Supply	+5V ±5%, Positive voltage for backplane and segments
6,7	S37,S38	Output	Segment Output to drive LCD display
8-21	S1 – S14	Output	Segment Output to drive LCD display
22	VEE	Power Supply	-3V ±5%, Negative voltage for backplane and segments. Connect to VSS for single supply operation .

PIN	SYMBOL	FUNCTION	DESCRIPTION
23-27	S15 – S19	Output	Segment Output to drive LCD display
28	BPOUT	Output	Backplane output to LCD display
29	T1	Logic Input	Controls LCD display under test mode. (Low for normal operation)
30	T2	Logic Input	Control LCD display under test mode. (Low for normal operation)
32	DOUT38	Logic Output	38th bit stage of the shift register. Used for cascading multiple devices.
33-49	S20 – S36	Output	Segment Output to drive LCD display
50	VSS	Power Supply	0V (Ground logic supply)
51	CSN	Logic Output	Chip select (Active Low)
52	CLN	Logic Output	Serial data input clock (Active Low)

Functional Description

Input Logic

Data is clocked into a serial shift register through the DIN input on the negative edge of CLN while CSN is held low. LD is normally held low until all the bits have been shifted into the register, then LD is pulsed high in order to parallel load the data to the segment outputs. CSN must be low when LD is pulsed. Latches are transparent while LD is high. A logic "1" in the shift register makes the corresponding segment on the output to be out of phase with respect to BPOUT. All logic inputs are CMOS compatible.

BPOSC and BPIN

The refresh rate for the segments and the backplane are determined by the frequency generated or injected in these two pins. The user can opt to force an external frequency into pin BPIN or use the internal frequency generator. To use the internal oscillator, BPIN and BPOSC are connected together and the appropriate RC network is connected to these pins according to Figure 1. The backplane frequency can be approximately calculated by:

$$f_{BP} \approx \frac{1}{256\,RC}$$ **(R = 220K ohm, C = 220pF, $f_{BP} \approx$ 80 to100 Hz.)**

When an external clock is used, apply the appropriate clock (square-wave) to the BPIN and leave the BPOSC open.

VEE Pin

VEE is a negative power supply voltage. V_{DD}-V_{EE} determines the LCD drive voltage amplitude for every segment and for the backplane. The FMD68151 is intended for driving low voltage displays (twisted nematic LCDs) in direct drive mode. Depending on the application, this pin can be biased anywhere between 0V and -3V.

DOUT

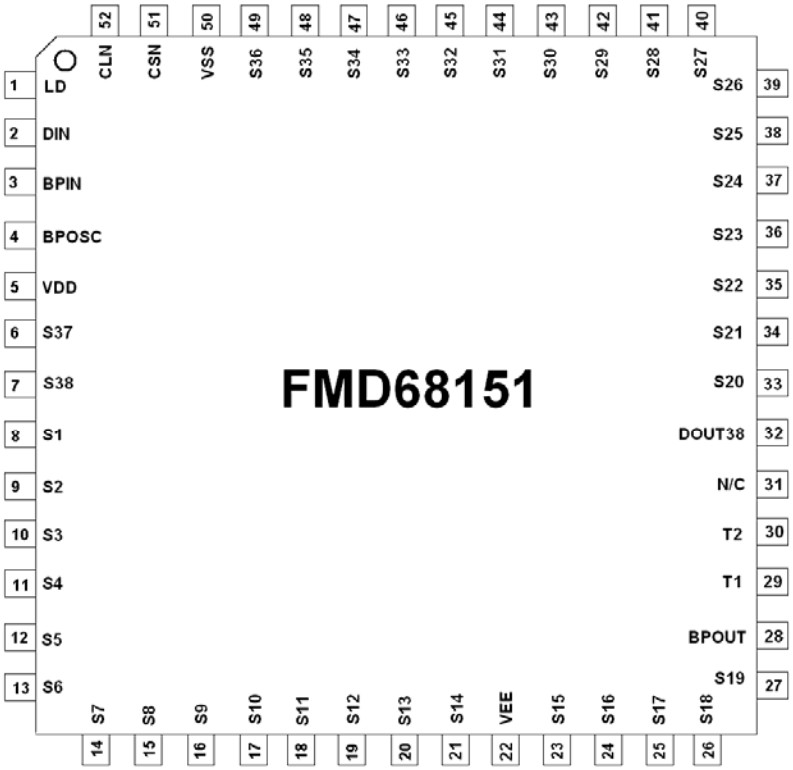
The DOUT38 pin is available for cascading devices to drive more segments (See Figure 2). This pin can also be used for verifying the integrity of the serial shift register data. This output can drive up to a 4mA load. The DOUT38 output changes on the positive edge of CLN. Devices with the 32nd. or the 30th. shift register data taps are also available.

Test Inputs

Test Mode	T1	T2	Display Mode
Normal operation	0	0	Normal
All Segments and BP in phase	1	0	All OFF
All Segments and BP out of phase	0	1	All ON
Segments Alternating ON / OFF	1	1	Even ON, Odd OFF

Test inputs are CMOS compatible.

Pin Configurations

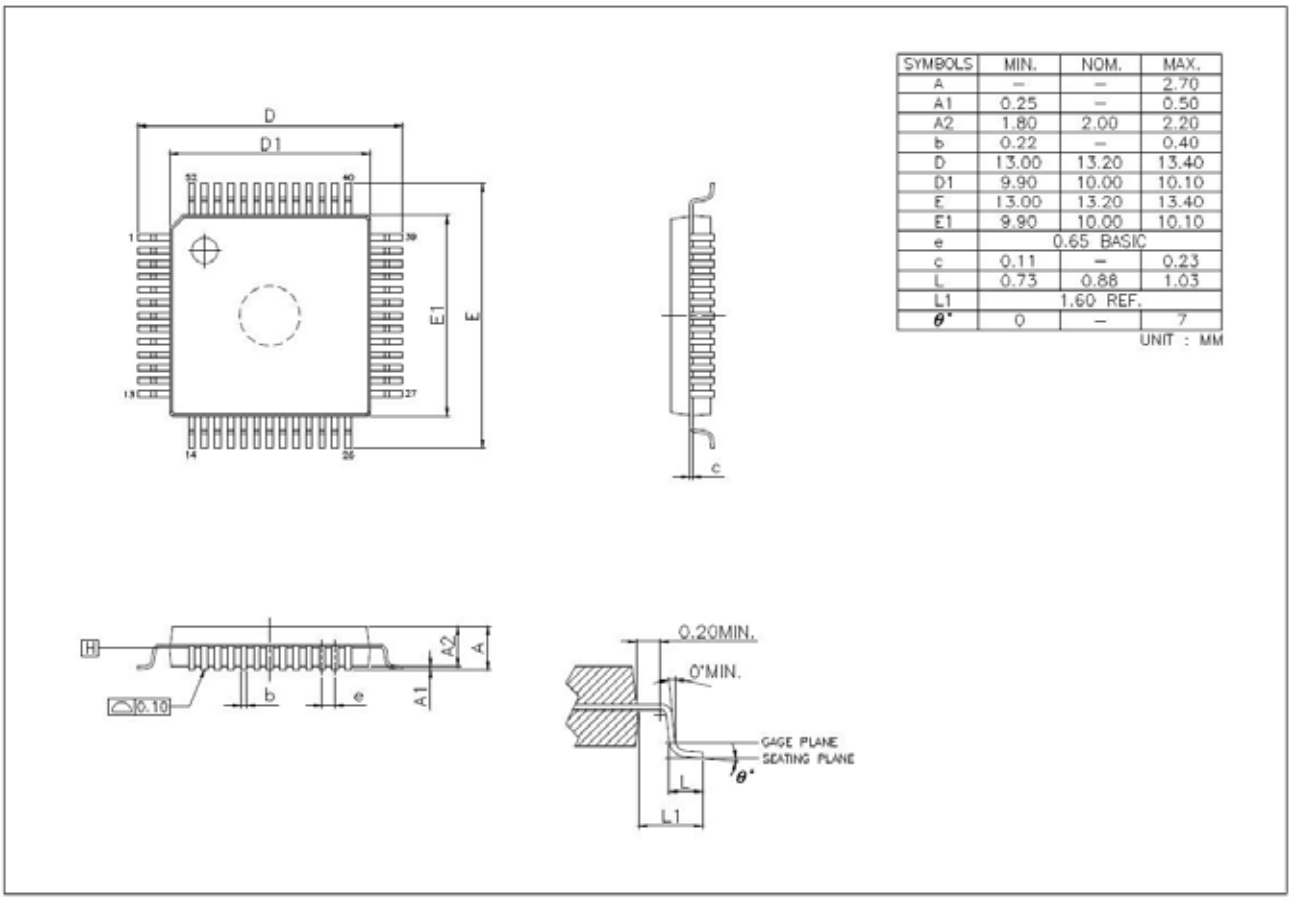


52 Pin Plastic PQFP package

Ordering Information

Part Number	Test Outputs	Number of Segments	DOUT Number	Package Type
FMD68151PQI	Yes	38	38	52-Pin PQFP
FMD68151PQI-32	Yes	38	32	52-Pin PQFP
FMD68151PQI-30	Yes	38	30	52-Pin PQFP

52-Pin Plastic Quad Flat Pack (PQFP) Package



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	2.70
A1	0.25	–	0.50
A2	1.80	2.00	2.20
b	0.22	–	0.40
D	13.00	13.20	13.40
D1	9.90	10.00	10.10
E	13.00	13.20	13.40
E1	9.90	10.00	10.10
e	0.65 BASIC		
c	0.11	–	0.23
L	0.73	0.88	1.03
L1	1.60 REF.		
θ°	0	–	7

UNIT : MM